What is Claimed is:

- A packet processing circuit comprising:
- a plurality of macros each of which processes
- 3 packet data on the basis of a clock and outputs the
- 4 processed packet data from at least one route, said
- 5 macros being cascade-connected; and
- a clock supply unit which supplies the clock
- 7 to a macro to be controlled and, when no packet data is
- 8 output for a predetermined time from all routes of a
- 9 macro on an input side of said macro to be controlled,
- 10 stops supplying the clock to said macro to be
- 11 controlled.
 - 2. A circuit according to claim 1, wherein said
 - 2 clock supply unit comprises
 - a clock buffer which supplies the clock to
 - 4 said macro to be controlled, and
 - 5 a clock management unit which causes said
 - 6 clock buffer corresponding to said macro to be
 - 7 controlled to stop supplying the clock when no packet
 - 8 data is output for the predetermined time from all the
- 9 routes of said macro on the input side of said macro to
- 10 be controlled.
 - 3. A circuit according to claim 2, wherein
 - 2 said macro on the input side comprises a first

- 3 signal output unit which outputs, to said clock
- 4 management unit, a first packet output notification
- 5 signal which indicates that the packet data is output,
- 6 and
- 7 said clock management unit comprises a packet
- 8 output detection unit which causes said clock buffer to
- 9 start supplying the clock when the first packet output
- 10 notification signal is enabled and stop supplying the
- 11 clock when the first packet output notification signal
- 12 is not enabled again within the predetermined time.
 - 4. A circuit according to claim 3, wherein said
 - 2 packet output detection unit comprises a counter circuit
 - 3 which detects the predetermined time by counting the
 - 4 number of clocks, said counter circuit resetting a count
 - 5 value when the first packet output notification signal
 - 6 is turned on.
 - 5. A circuit according to claim 4, wherein said
 - 2 counter circuit detects the predetermined time by
 - 3 counting the number of clocks necessary until the packet
 - 4 data passes through said macro on the input side.
 - 6. A circuit according to claim 3, wherein
 - 2 said macro on the input side comprises a
 - 3 plurality of routes to output the processed packet data,
 - 4 and

- 5 said first signal output unit outputs, to said
- 6 clock management unit, a first packet output
- 7 notification signal which indicates that the packet data
- 8 is output from at least one of the routes.
 - 7. A circuit according to claim 6, wherein
- 2 said macro on the input side comprises a
- 3 second signal output unit which outputs, to said first
- 4 signal output unit for each of the routes, a second
- 5 packet output notification signal which indicates that
- 6 the packet data is output, and
- 7 said first signal output unit comprises a gate
- 8 circuit which generates the first packet output
- 9 notification signal by ORing the received second packet
- 10 output notification signal.